Summary of changes from DFI 2.1 to DFI 3.0

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The following list provides a summary of changes in the DFI specification transitioning from version 2.1 to version 3.0. This list is not comprehensive and should be used in conjunction with the DFI 3.0 Specification. Also note that the DFI 3.0 specification received significant rewording and reformatting to improve accessibility and clarity of information.

- Read leveling (DQ data eye and DQ gate training)
  - MC evaluation support has been removed
    - In practice, the sequences necessary for finding the correct delay programming values for the DLL’s within the PHY is not universally common between PHY implementations.
    - These sequences may encounter various boundary conditions within the PHY requiring unique adjustments specific to the implementation.
    - Continuing to support MC Evaluation mode as a required feature in all MC’s is a significant effort. Newly defined functions including new memory technologies, multiple CS training, etc. continue to create additional scenarios that need to be comprehended.
  - Pattern encoding
    - Added dfi_lvl_pattern signal to communicate pattern sequences between the MC and PHY. Pattern encodings are defined per DRAM technology.

- The dfi_rdlvl_mode, dfi_rdlvl_gate_mode, and dfi_wrlvl_mode signals have been replaced by programmable parameters PHY_RDLVL_EN, PHY_RDLVL_GATE_EN, and PHY_WRLVL_EN.
  - DFI 2.1 defined 4 modes: No support, Independent, PHY Eval, and MC Eval.
  - DFI 3.1 defines 2 modes: enabled and disabled.

- New periodic training flag
  - A new signal, dfi_lvl_periodic, has been defined indicating whether the current training operation is full training or periodic training.
  - Required for the MC, optional for the PHY.

- Support for refresh and non-data commands during training
  - In some systems, training may take a long time. Added a sequence for executing non-data commands (refresh, precharge) during the training sequence.
  - Support required for both the MC and PHY.

- Multiple chip select training
  - Added support for dfi_wrdata_cs_n and dfi_rddata_cs_n to the training sequence.
  - Added dfi_phy_rdlvl_cs_n, dfi_phy_rdlvl_gate_cs_n, and dfi_phy_wrlvl_cs_n to allow the PHY to indicate a target chip select when requesting training.

- Independent timing of DFI read data valid per data slice
  - In DFI 2.1, the dfi_rddata_valid signal was required to be returned in sync from all PHY data slices.
In DFI 3.0, the dfi_rddata_valid signal is allowed to be returned independently. The MC will combine the DFI read data words.

- Data path chip selects
  - DFI 2.1 only communicates the chip select information on the dfi_cs_n signal.
  - DFI 3.0 adds new data path chip select signals and associated timing parameter:
    dfi_wrdata_cs_n, dfi_rddata_cs_n, tPHY_WRCSLAT, tPHY_RDCSLAT, tPHY_WRCSGAP, and tPHY_RDCSGAP.
  - Data path chip selects are optional for both the MC and PHY.
  - Data path chip selects are applicable to PHYs that support unique timing per chip select.

- Error interface
  - A new error interface added to communicate error information from the PHY to the MC.
  - New signals: dfi_error and dfi_error_info
  - Support is optional for both the MC and PHY.

- Remove tPHY_WRDELAY timing parameter
  - This timing parameter allowed the MC operating in frequency ratio system to align write data to phase 0 and require the PHY to add clock stages required for proper command to data alignment. Removed because (a) not necessary, MC can do the alignment and (b) interoperability - most PHYs do not implement this required function.

- Update interface enhancements
  - Clarifications to usage model.

- Idle bus definition
  - New timing parameter tWRDATA_DELAY defined to define when a DFI write command is complete as required by clarification of when the DFI bus is in the IDLE state.

- Read data rotation

- Read data pointer resynchronization
  - Read data pointers resynchronized on assertion of either dfi_ctrlupd_req or dfi_phyupd_ack.

- Support for DDR4 memory
  - CRC support
    - Write data only
    - CRC can be generated and checked in MC or PHY
    - Support is optional
  - Command/Address parity timing
    - DFI 2.1 defines a fixed timing relationship between dfi_cs_n and dfi_parity_in.
    - DFI 3.0 adds a new timing parameter which defines relationship between dfi_cs_n and dfi_parity_in. This signal is driven from the MC to the PHY.
  - CRC and Command/Address parity errors
    - DFI 2.1 reports parity errors on the dfi_parity_error signal
    - DFI 3.0 replaces the dfi_parity_error signal with the active low dfi_alert_n_aN signal. This signal is driven from the PHY to the MC.
The dfi_alert_n_aN signal is a phased signal to communicate to the MC the number of DRAM clocks the signal is asserted.

The dfi_alert_n_aN signal timing is defined by both tPHY_CRCMAX_LAT and tPHY_CRCMIN_LAT which allows more accurate association of the error to the failing command. Accurate association of the error to the command is an optional feature.

DDR4 reports both CRC and CA parity errors on a shared signal.

Support is optional for the PHY, required for the MC.

- **Data Bus Inversion (DBI)**
  - DBI support is optional for both the MC and the PHY. If supported, both modes must be supported by the MC; at least one mode must be supported by the PHY.
  - The data inversion may be done in either the MC or the PHY. This is defined by PHY_DBI_MODE.
  - When DBI mode is enabled (either mode), write data masking is not supported. This is a DRAM limitation.

- **Read leveling – read data eye training and DQS gate training**
  - DDR4 adds support for several different read data patterns and formats. This information is encoded on the new dfi lvl_pattern signal.

- **New CA signals and CA signal extensions**
  - Added DDR4 command signals: dfi_act_n, dfi_bg, and dfi_cid.
  - Added DDR4 command extensions:
    - The dfi_ras_n, dfi_cas_n, dfi_we_n signals mapped to A16, A15, A14 during ACT command.
    - The dfi_address[16:14] not used for DDR4 accesses.

- **New CA timing parameter: tCMD_LAT**
  - New timing parameter, tCMD_LAT, defines the timing relationship between dfi_cs_n and when the command/address bus is driven.

- **The dfi_wrdata_en signal definition modified**
  - The dfi_wrdata_en signal definition has been modified to support new commands such as per-DRAM addressability, a new feature of DDR4 DRAMs.

- **New features that did not require modifications to the specification**
  - VREF training
  - Write and read command preambles.

- **New features not defined**
  - Geardown mode