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bits of the _____ work independently and individually
index register | base register | **flags register** | accumulator
My Ok | Page # 12

Motorola 68K processors have _____ 23bit general purpose registers.
64 | 8 | **16** | 32
My Ok | Page # 191

Video services are classified into _____broad categories
2 | 3 | 4 | 5
My Ok | Page # 149

In device attribute word which of the following bit decides whether it is a character device or a block device
Bit 12 | Bit 13 | Bit 14 | **Bit 15**
My Ok | Page # 166

The programmable interval timer (PIT) has input frequency of
►**1.193MHZ** | ►2.193 MHZ | ►3.193 MHZ | ►4.193MHZ
My Ok | Page 122

The input frequency of the programmable interval timer (PIT) is
Fixed | Depends on processor clock | Variable | Depends on hardware attached
My Ok | Page # 122

Memory address space is selected when which of the following instructions is given to the processor
MOV | DEC | IN | ADD
My Ok | Page # 115

BPB stands for
Basic parameter block | Bios precise block | Basic precise block | **Bios parameter block**
My Ok | Page # 166

"INT13 --BIOS disk services" generally uses which register to return the 'error flag'?
CF | DL | AH | AL
My Ok | Page # 156

"INT13 --BIOS disk services" generally uses which register to return the 'error code'?
CF | DL | **AH** | AL
My Ok | Page # 156

The first sector on the hard disk contains the
Hard disk size | **Partition table** | Data size | Sector size
My Ok | Page # 158

Operating system organize data in the form of
Folder | Batch file | File | None of above
My Ok

Device derive can be divided into ----------major categories.
5 | 4 | 3 | **2**
My Ok

BL contains 5 decimal then after right shift , BL will become
3 | 2.5 | 5 | 10
My Ok | Page # 52 | right shift is division by 2

INT 10 is used for……services.
RAM | Disk | **BIOS video** | DOS video
My Ok | Page # 108

Priority of IRQ 0 interrupt is
Medium | high | **highest** | low
My Ok | Page # 114

IRQ 0 has priority

Low High ***Highest*** Medium
My Ok Page # 114

IRQ with highest priority is
Keyboard IRQ ***Timer IRQ*** Sound Card Floppy Disk
My Ok Page # 114

Which of the following interrupt is of highest priority interrupt?
Key board interrupt INT3 INT 2 **Timer interrupt**
My Ok Page # 114

Threads can have function calls, parameters and _____variables.
Global **local** legal illegal
My Ok page # 141

How many prevalent calling conventions do exist
1 **2** 3 4

In Assembly language programming, how many prevalent calling conventions do exist
1 **2** 3 4
My Ok Page # 187

Which of the following is a special type of interrupt that returns to the same instruction instead of the next instruction?
Divide overflow interrupt Debug interrupt
Arithmetic overflow interrupt Change of sign interrupt
My Ok Page # 107

Which of the following IRQs is derived by a timer device?
IRQ 0 IRQ 1 IRQ 2 IRQ 3
My Ok Page # 113

Which of the following IRQs is derived by a key board?
► IRQ 0 **► IRQ 1** ► IRQ 2 ► IRQ 3
My Ok Page # 114

Which of the following interrupts is used for Arithmetic overflow?
INT 1 INT 2 INT 3 **INT 4**
My Ok Page # 106

Which of the following IRQs is connected to serial port COM 2?
IRQ 0 IRQ 1 IRQ 2 **IRQ 3**
My Ok Page # 114

Which of the following IRQs is connected to serial port COM 1?
► IRQ 4 ► IRQ 5 ► IRQ 6 ► IRQ 7
My Ok Page # 114

An End of Interrupt (EOI) signal is sent by
Handler Processor IRQ PIC
My Ok Page # 114

The source registers in OUT is
AL or AX BL or BX CL or CX DL or DX
My Ok Page # 115

In programmable interrupt controller which of the following ports is used for selectively enabling or disabling interrupts
19 20 **21** 22
My Ok Page # 115

In programmable interrupt controller which of the following ports is referred as a control port?
19 **20** 21 22
My Ok Page # 115

In programmable interrupt controller, which of the following ports is referred as interrupt mask register?
19 20 **21** 22
My Ok Page # 115

The number of pins in a parallel port connector are
25 30 35
My Ok Page # 125

Which of the following pins of a parallel port connector are grounded?
10-18 **18-25** 25-32 32-39
My Ok Page # 125

Programmable interrupt controller has two ports 20 and 21. Port 20 is the control port while port 21 is.....
The Interrupt mask register Interrupt port
Output port Input port
My Ok Page # 115

Programmable Interrupt Controller (PIC) has
► One input signals and eight output signals ► One input signal and one output signal
► **Eight input signals and one output signals** ► Eight input signals and eight output signals
My Ok Page # 113

A 32bit address register can access upto .....of memory so memory access has increased a lot.
2GB **4GB** 6GB 8GB
My Ok Page # 175

In NASM an imported symbol is declared with the ____while and exported symbol is declared with the ____
Global directive, External directive **External directive, Global directive**
Home Directive, Foreign Directive Foreign Directive, Home Directive
My Ok Page # 189

Single step interrupt is
Hardware interrupt **Like divide by zero interrupt**
Like divide by 1 interrupt Software interrupt
My Ok Page # 133

Sun SPARC Processor has a fixed _____ instruction size.
16-bit **32-bit** 64-bit 20-bit
My Ok Page # 192

IDT stands for _____.
interrupt descriptor table individual descriptor table
inline data table None of the above
My Ok Page # 182

Size mismatch error is a syntex error
True **false**
My Ok

Memory to memory operation is allowed
True **false**
My Ok Page # 29

Register to register operation is not allowed
true **flase**
My Ok Page # 29

Suppose al contain 5 decimal then after two left shift the value of al is
5 **10** 20 15
My Ok Page # 52 left shift is multiplication by 2

The interrupt call loads new values in CS, IP and _____ registers.
► DS ► SS **► FLAGS** ► BP
My Ok Page # 103

After the execution of PUSH statement, what will happen ?
► SP is increased by 1 ► SP is decreased by 1
► SP is increased by 2 **► SP is decreased by 2**
MY Ok Page # 68

What is the size of a Sector of a standard 1.44MB Floppy disk having 80 tracks and 18 Sectors/track?
► 128 Bytes ► 256 Bytes **► 512 Bytes** ► 1024 Bytes

The thread registration code initializes the PCB and adds it to the linked list. so that which will give it a turn?
► scheduler ► linker ► debugger ► assembler
My Ok Page # 141

The no -2 is represented in word as
0002 0200 **FFFE** EFFF
My Ok Page # 39

After execution of instruction RET, SP is
Increment by 2 Increment by 1 Decrement by 2 Decrement by 1
My Ok Page # 72

LODS instruction transfer a byte or word from source to _____
AL or AX register BL or BX register CL or CX register DL or DX register
My Ok Page # 91

Which of the following IRQs is used for sound card or network card?
IRQ3 IRQ4 **IRQ5** IRQ6
My Ok Page # 106

Operation of CMP is to subtract
Source from destination Destination from source
Add 1 to destination Add source and destination
My Ok page 85

The operation of CMP is to subtract source from destination
True False
My Ok page 85

After execution of CMP instruction the content of_____
Source change Destination change
Both (source and destination) change **Source and destination donot change**
My Ok page 85

AX=5, BX=5, CF and ZF is set, AF and DX contain zero then after execution of instruction, ADC AX, BX, AX will contain value_____
5 **10** 11 12

Which of the following flag is affected by MOVSW?
PF DF ZF **No effect on flags**
My Ok **Click Here**

Sign flag is set to _____ for positive numbers.
0 +1 0 or 1 1
Page # 9

INT 10 used for _____
BIOS video DOS video RAM DISK
page # 141

_____ not use for mathematical operation.
Direction, interrupt, trap flag

VESA VBE standard for_____
Ultra resolution mode Medium resolution mode
Low resolution mode **high resolution modes**
page 172

VESA stands for_____
Variable Electronics Standards Association **Video Electronics Standards Association**
Video Energy Standards Association Vega Energy Standards Association
page 172

IDTR is _____ register.
16 bit 20 bit 32 bit **48 bit**
Page # 174

In computer architecture, CISC stands for _____.
Complex instruction set computer Complex instruction system computer
Correct instruction set computer Correct instruction system computer

In multi-tasking, which is called scheduler for saving and restoring the register?
INT10 INT09 **INT08** INT07

In multi-tasking programming, all threads are
Independent to each other Dependent to each other Not scheduled Not executed
page 135

"INT10, video scroll up window" is a type of video service used in which mode?
Numeric Graphic **Text** Audio

8088 is _____ processor.
16 bits 32 bits 64 bits 128 bits
Page # 167

AX register is extended 32 bit register is renamed as_____
AXE **EAX** AAX XAX
Page # 167

IN 68k processor there is _____ program counter (PC) that holds the address of currently executing instruction.
8 bits 16 bits **32 bits** 64 bits
Page 183

An 8x16 font is stored in _____ bytes.
8 **16** 4 2
Page # 142

The IN instruction uses _____ as destination registers.
AL, AX BL, BX CL, CX DL, DX
Page # 107

Which is Non-maskable interrupt?
INT2 INT3 INT1 INT0

Which is arithmetic overflow interrupt?
INT4 INT3 INT5 INT2
Page # 98

In PIC, control port is
20 19 21 22
Page #107

VESA VBE 2.0 is a standard for
► **High resolution Mode** ► Low resolution Mode
► Medium resolution Mode ► Very High resolution Mode

Which of the following gives the more logical view of the storage medium
► BIOS ► **DOS** ► Both ► None
153page

The physical address of IDT(Interrupt Descriptor Table) is stored in _____
► GDTR ► **IDTR** ► IVT ► IDTT
PAGE # 174

For the execution of the instruction "DIV BL", the implied dividend will be stored in
► **AX** ► BX ► CX ► DX
Page # 85

INT 21 service 01H is used to read character from standard input with echo. It returns the result in _____ register.

► **AL** ► BL ► CL ► BH

Page # 144

BIOS sees the disks as

► Logical storage device ► **Raw storage device**

► In the form of sectors only ► In the form of tracks only

Page # 148

Value of AH in the write Graphics pixel service is

► **0Ch** ► 0Bh ► 1Ch ► 2Ch

IRQ is referred to

► **Eight input signals** ► One output signal

► One input signals ► Eight output signals

Instruction Pointer holds the address of the

Previous instruction to be executed Current instruction

Next instruction to be executed None of the given

Register whose each bit specify a different meaning is

Accumulator Register Pointer Register

Index register **Flag register**

By default CS is associated with

SS BP CX **IP**

Unconditional jump can be

near short far **all of the given**

Register are storage cell

Outside the processor Both inside and outside the processor

Inside the processor None of the given

Unconditional jump

Execute in every condition whether true or false **If the condition is true**

If the condition is false None of the given

Which type of Rotation it is "Every bit moves one position to the right and the bit dropped from the right is inserted at the left. This bit is also copied into the carry flag."

ROL **RCR** RCL None of the given

Assembly language is not a low level language.

True **False**

Group of bits processor uses to inform memory which element to read/write is collectively known as

Control bus Data bus Address bus RAM

90 is the op-code of

Do nothing Add Subtract Multiplication

My Ok Page # 22

We cannot add two base register i.e. (bx+bp) or can't use in an instruction

True False

Intel follow

Littel endian Big endian

Both littel endian and big endian None of the given

SHL and SAL are same

True False

My Ok Page # 52

The first 16-bit processor produced by "Intel" was 8085

True **False**

It was 8088

The extension of assembly language file is

.doc .com .lst **.asm**

When a large number is subtracted from a smaller number, a borrow is needed; in this case which flag will be set

ZF **CF** SF OF

All the addressing mechanisms in iAPX88 return a number called _____ address.

Effective address Physical address Direct address None of the given

Which type of shifting is "Inserts a zero from the left and moves every bit one position to the right and copies the rightmost bit in the carry flag."

SHL SAL SAR **None of the given**

The SHR inserts a zero from the left and moves every bit one position to the right and copy the rightmost bit in the carry flag.

mov [1234], ax is an example of

Direct addressing Base register indirect

Base+index None of the given

Leture # 8 Ok

Registers are also called scratch pad ram

True False

The basic function of register is to?

Hold the operand Hold the operator

Hold both the operator and operand None of the given

The jump is taken if the last arithmetic operation changed the sign unexpectedly.

JO JNO JNZ JZ

This jump is taken if the last arithmetic operation produced a number in its destination that has even parity, which jump is taken

JP **JPE** JNP Both JP and JPE

This jump is taken if the last arithmetic operation produced a number in its destination that has even parity

JP ***JPE*** *JNP* *None*

In JA jump is not taken after a CMP if the unsigned destination is larger than the unsigned source.

True **False**

My Ok Page # 42

Which type of rotation it is "The carry flag is inserted from the left, every bit moves one position to the right, and the right most bit is dropped in the carry flag. "

RCR ROL RCL ROR

In direct addressing the memory address given in the instruction is

Fixed Variable Register Empty

We cannot Subtract index register from the base register (bx-si)in assembly language

True False

The execution of the instruction "mov word [ES: 160], 0x1230" will print a character on the screen at:

First column of second row Second column of first row

Second column of second row First column of third row

Which type of shif operation it is "The zero bit is inserted from the right and every bit moves one position to its left with the most significant bit dropping into the carry flag"

shl sal sar **both shl and sal**

My Ok Page # 52

SP is associated with……. By default

► **SS** ► DS ► CS ► ES

Page # 26

Which bit of the attributes byte represents the red component of foreground color

► 5 ► 4 ► 3 **► 2**

Page # 73

Which bit of the attributes byte represents the red component of background color ?
► 3 ► 4 ► 5 **► 6**
Page # 73

Which bit of attributes byte represents the blue component of foreground color?
0 1 2 3

In DOS input buffer, the number of characters actually read on return is stored in _____ byte.
► third ► fourth ► first **► second**
Page # 144

In STOSW instructions, when DF is clear, SI is
► Incremented by 1 **► Incremented by 2**
► Decremented by 1 ► Decremented by 2

In STOSB instruction, when DF is clear, SI is
Incremented by 1 Incremented by 2 Decremented by 1 Decremented by 2

In STOSB instructions, SI is decremented or incremented by
► 3 ► 2 **► 1** ► 4

In STOSW instruction , When DI is cleared , SI is
Incremented by 1 ***Incremented by 2***
Decremented by 1 Decremented by 2

Which of the following interrupts is Non makeable interrupt
► INT 2 ► INT 3 ► INT 0 ► INT 1
PAGE # 97

The time interval between two timer ticks is ?
► 40ms ► 45ms ► 50ms **► 55ms**
PAGE # 114

In 68K processors there is a 32bit ..... that holds the address of currently executing instruction
► Program counter ► Stack pointer ► Register ► Stack
PAGE 184

In 68K processors there is a ..... program counter (PC) that holds the address of currently executing instruction
► 16bit **► 32bit** ► 64bit
183page

Which of the following is NOT true about registers?
► Their operation is very much like memory ► Intermediate results may also be stored in registers
► They are also called scratch pad ram **► None of given options**

Types of jump are:
► Short, near **► short, near, far** ► Near, far ► short, far
PAGE # 37

MS DOS uses ____ display mode.
► Character based ► Graphics based ► Numeric based ► Console based
Page # 72

The table index (TI) is set to _____ to access the GDT (Global Descriptor Table).
► 1 **► 0** ► -1 ► -2
Page # 168

VESA (Video Electronics Standards Association) organizes 16 color bits for every pixel in_____ format
► 5:5:5 formats **► 5:6:5 format** ► 6:5:6 formats ► 5:6:7 formats
Page # 172

Which flags are NOT used for mathematical operations ?
► Carry, Interrupt and Trap flag. **► Direction, Interrupt and Trap flag.**
► Direction, Overflow and Trap flag. ► Direction, Interrupt and Sign flag.
Page # 126

_____are NOT used for mathematical operations ?
► Carry, Interrupt and Trap flag. ► **Direction, Interrupt and Trap flag.**
► Direction, Overflow and Trap flag. ► Direction, Interrupt and Sign flag.
Page # 126

Direction flag, the interrupt flag, and the trap flag are
Used for mathematical operations **not used for mathematical operations**
status flags not status flags

Suppose AL contains 5 decimal then after two left shifts produces the value as
► 5 ► 10 ► 15 ► **20**
My Ok Left shift is multiplication by 2

In graphics mode a location in video memory corresponds to a _____ on the screen.
► Line ► **Dot** ► Circle ► Rectangle
page 142

Creation of threads can be
► static ► **dynamic** ► easy ► difficult
Page # 133

Which of the following IRQs is used for Floppy disk drive?
► IRQ 4 ► IRQ 5 ► **IRQ 6** ► IRQ 7
page 106

Which of the following IRQs is used by the parallel port?
IRQ 5 IRQ 4 IRQ 6 **IRQ 7**

To reserve 8-bits in memory ___ directive is used.
► **db** ► dw ► dn ► dd
Page # 17

In the "mov ax, 5" 5 is the _____ operand.
► **source** ► destination ► memory ► register

RETF will pop the segment address in the
► **CS register** ► DS register ► SS register ► ES register
Page # 61

RETF will pop the offset in the
► BP ► **IP** ► SP ► SI

When a number is divided by zero"A Division by 0" interrupt is generated. Which instruction is used for this purpose?
► INT 0 ► INT 1 ► INT 2
► **This interrupt is generated automatically**

When two devices in the system want to use the same IRQ line then what will happen?
► An IRQ Collision ► **An IRQ Conflict** ► An IRQ Crash ► An IRQ Blockage
Page # 114

If two devices uses same IRQ then there is
IRQ collision **IRQ conflict** IRQ drop

In the instruction **MOV AX, 5** the number of operands are
► **1** ► 2 ► 3 ► 4

move [bp], al moves the one byte content of the AL register to the address contained in BP register in the current
Stack segment Code segment Data segment Extra segment
Page # 27

In a rotate through carry right (RCR) instruction applied on a 16 bit word effectively there is
16 bits rotation 1 bit rotation **17 bits rotation** 8 bits rotation
Page # 45

The 8088 stack works on
Word sized elements Byte sized elements
Double sized element Nibble sized element
Page # 60

Suppose a decimal number 35 when its binary is shifted to write two places the new number will become
35 70 **140** 17

The physical address of the stack is obtained by
► SS:SI combination ► **SS:SP combination**
► ES:BP combination ► ES:SP combination

The serial port connection is a ---------- connector
► **9pin DB 9** ► 8pin DB 9 ► 3pin DB 9 ► 9pin DB 5
Page # 171

After the execution of STOSW, the CX will be
► **Decremented by 1** ► Decremented by 2
► Incremented by 1 ► Incremented by 2

Assembly language is:
► **Low-level programming language** ► High-level programming language
► Also known as machine language ► Not considered closer to the computer

The number of bits required to access 1MB of memory are
► 16 bits ► 32 bits ► **Depends on the processor architecture** ► 20 bits

mov [si+300], ax is an example of indexed register indirect +offset
True False

BP by difficult associated with _____
CS IP **SS** SP
My Ok Page # 34

Register to memory operation is not allowed
True **False**

address is always go from
Processor to memory Memory to processor
Memory to Memory Non of the Given

Data Bus is _____
Uni-directional **Bi-directional** Non-directional Non of the given option

Data bus is bidirectional because_____
To way **Data moves from both, processor to memory and memory to processor,**
None of the Given Data moves from both, processor to memory and memory to data Bus,

iAPX88 architecture consist of _____
14 register 16 register 32 register Non of the give
Naq main register kay name

All the addressing mechanism in iAPX returns a number called _____ address.
Effective address Physical address Direct address Non of the given
My Ok Page # 33

Motorola Follow
Big endian Litter endian Both of them Non of the given

Registered is also called scratch pad ram
True False

CX register mostly use in
Counter Register Flag Register Base Register Distention Register

Memory cell can not be wider the data bus.
True False

The iAPX88 processor supports _____modes of memory access.
6 ***7*** *8* *9*

In JZ jump is not taken if the last arithmetic operation produced a zero in its destination.
True ***False***

Physical address calculation depends on
Base address ***Effective address*** *Offset Address* *None of the above*

The other directive is "define word" or "dw" with the same syntax as "db" but reserving a whole word of __ bits instead of a byte.
32 *8* ***16*** *64*

SI or DI is used we name the method.
Based Addressing ***Indexed Addressing*** *Stack Addressing* *None of the above*

FLAG register in Intel x86 microprocessors that contains the current state of the processor
True *False*

The addressing method that can be used to access a two dimensional array is.
Base + Index + Offset addressing ***Base + Index addressing***

Constant is never use as a
Source **Destination** *Both as source and destination* *None of the given*

BX is a register in which intermediate arithmetic and logic results are stored.
True ***False***

The process through which the segment register can be explicitly specified is known as
Segment Addressing *Segment Override Prefix*
Segment Indexing *None of the above*

MOV AL,BX is a type of ___ error.
Syntax ***size mismatch error*** *size mismatch*

Mechanism used to drop carry for making the calculated address valid is known as:
Carry Overload *Overflow* ***Address Wraparound*** *None of the above*

Simple CMP instruction uses _____ operation
Addition *Division* ***Subtraction*** *Multiplicaion*

SS is by default associated with
BP *IP* *SP* ***BP***

When a 32 bit number is divided by a 16 bit number, the remainder is of
4 bits *8 bits* ***16 bits*** *32 bits*

When a 32 bit number is divided by a 16 bit number, the quotient is of
► **4 bits** ► 32 bits ► 16 bits ► 8 bits

Register to constant data movement is allowed?
No *Yes*

DOS has a single entry point through ------- just like a pin hole camera
INT 21

After the execution of instruction "RET "
► **SP is incremented by 2** ► SP is decremented by 2
► SP is incremented by 1 ► SP is decremented by 1

After the execution of instruction "RET 2"
► SP is incremented by 2 ► SP is decremented by 2
► **SP is incremented by 4** ► SP is decremented by 4

The second byte in the word designated for one screen location holds
The dimensions of the screen | Character position on the screen
Character color on the screen | ASCII code of the character

In the word designated for one screen location, the higher address contains
► **The character code** | ► The attribute byte
► The parameters | ► The dimensions

REP will always
Increment CX by 1 | Increment CX by 2
Decrement CX by 1 | Decrement CX by 2

The basic function of SCAS instruction is to
Compare | Scan | Sort | Move data

Index registers are used to store _____
Data | Intermediate result | Address | Both data and addresses

To convert any digit to its ASCII representation
Add 0x30 in the digit | Subtract 0x30 from the digit
Add 0x61 in the digit | Subtract 0x61 from the digit

Which mathematical operation is dominant during the execution of SCAS instruction
Division | Multiplication | Addition | Subtraction

If AX contains decimal -2 and BX contains decimal 2 then after the execution of instructions: CMP AX, BX
JA label
Jump will be taken | Zero flag will set | ZF will contain value -4 | Jump will not be taken

If the direction of the processing of a string is from higher addresses towards lower addresses then
ZF is cleared | DF is cleared | ZF is set | DF is set

The instruction ADC has_____ Operand(s)
0 | 1 | 2 | 3

The clear screen operation initializes the whole block of video memory to:
0417 | 0714 | **0741** | 0720

When the operand of DIV instruction is of 16 bit then implied dividend will be of
64-bit | **32-bits** | 16-bits | 8--bits

Which of the following is the pair of register used to access memory in string instruction:
DI and BP | SI and BP | **DI and SI** | DS and Si

We can access the DOS service using;
Int 0x21 | Int 0x13 | Int 0x 10 | Int 0x 08

VESA VEB 2.0 is standard for
High Resolution Mode | Low Resolution Mode
Very High Resolution Mode | Medium Resolution Mode

To clear direction flag which instruction is used
Cld | Clrd | Cl df | Clr df

Interrupt that is used in debugging with help of trap flag is
INT 0 | ***INT 1*** | INT 2 | INT 3

Which of the following interrupt is used in debugging with the help of trap flag?
INT 0 | ***INT 1*** | INT 2 | INT 3

INT for arithmetic overflow is
INT 1 | INT 2 | INT 3 | ***INT 4***

IRQ referred as
Eight Input signals | One Input signal | Eight Output signals | One output signal

IRQ for keyboard is ____***1***_____

Pin for parallel port ground is
10-18 ***18-25*** 25-32 32-39

The physical address of Interrupt Descriptor Table (IDT) is stored in
GDTR ***IDTR*** IVT IDTT

The physical address of Interrupt Descriptor Table (IVT) is stored in
GDTR ***IDTR*** IVT IDTT

Execution of "RET 2" results in CX register is
Count register Data register Index register Base register

IN DB-9 connector the Data Set ready pin is at
5 ***6*** 7 8

IN 9 pin DB-9, which pin number is assigned to DSR (Data Set ready)
5 ***6*** 7 8

Division by zero is done by which interrupt.
Interrupt 0.
My Ok *Page # 85*

The routine that executes in response to an INT instruction is called
► ISR ► IRS ► ISP ► IRT
My Ok **Page # 103**

The first instruction of "COM" file must be at offset:
► 0x0010 **► 0x0100** ► 0x1000 ► 0x0000

"Far" jump is not position relative but is _____
► memory dependent **► Absolute** ► temporary ► indirect

Only _____ instructions allow moving data from memory to memory.
► string ► word ► indirect ► stack

DIV instruction has
► Two forms ► Three forms ► Four forms ► Five forms

When the operand of DIV instruction is of 16 bits then implied dividend will be of
► 8 bits ► 16 bits **► 32 bits** ► 64 bits

After the execution of MOVS instruction which of the following registers are updated
► SI only ► DI only **► SI and DI only** ► SI, DI and BP only

In 8088 architecture, whenever an element is pushed on the stack
► SP is decremeted by 1 **► SP is decremented by 2**
► SP is decremented by 3 ► SP is decremented by 4
My Ok

When a very large number is divided by very small number so that the quotient is larger than the space provided, this is called
► Divide logical error **► Divide overflow error**
► Divide syntax error ► An illegal instruction
My Ok

Which of the following options contain the set of instructions to open a window to the video memory?
► mov AX, 0xb008
mov ES, AX
► mov AX, 0xb800
mov ES, AX
► mov AX, 0x8b00
mov ES, AX
► mov AX, 0x800b
mov ES, AX

In a video memory, each screen location corresponds to
► One byte **► Two bytes** ► Four bytes ► Eight bytes

The execution of the instruction "mov word [ES : 0], 0x0741" will print character "A" on screen , background color of the screen will be

► Black ► White ► Red

Conditional jump can only:

Far **Short** Near all of the given

The 8088 processor divides interrupts into _____ classes?

2 3 4 5

My Ok Page # 103

The INT 0x13 service 0x03 is use to …

Read disk sector **Write disk sector** Reset disk sector Get drive parameters

BP by default associated with

CS IP **SS** SP

Stack is a _____ that behaves in a first in last out manner.

Program **data structure** Heap None of the Given

COM2 is connected with

IRQ 2 **IRQ 3** IRQ 4 IRQ 5

On executing INT 0x21 service 0x3D, if file is successfully opened

CF will contain 1 CF will contain 0 ZF will contain 1 ZF will contain 0

Hard disk MBR(Master Boot Record) is of size_____.

446 bytes 350 bytes 512 bytes 256 bytes

To transfer control back the RET instruction take

1 argument 1 argument 3 arguments **No arguments**

CMPS instruction subtracts the source location to the destination location. Destination location always lies in

DS:SI DS:DI ES:SI **ES:DI**

Regarding assembler, which statement is true:

Assembler converts mnemonics to the corresponding OPCODE

Assembler converts OPCODE to the corresponding mnemonics

Assembler executes the assembly code all at once

Assembler executes the assembly code step by step

If "BB" is the OPCODE of the instruction which states to "move a constant value to AX register", the hexadecimal representation (Using little Endian notation) of the instruction "Mov AX,336" ("150" in hexadecimal number system) will be:

0xBB0150 0x5001BB 0x01BB50 0xBB5001

The maximum parameters a subroutine can receive (with the help of registers) are

6 **7** 8 9

In assembly the CX register is used normally as a _____register.

source **counter** index pointer

Suppose the decimal number "35" after shifting its binary two bits to left, the new value becomes _____

35 70 **140** 17

When divide overflow occurs processor will be interrupted this type of interrupt is called

Hardware interrupt **Software interrupt**

Processor exception Logical interrupts

My Ok Page # 107

After the execution of SAR instruction

► The msb is replaced by a 0 ► The msb is replaced by 1

► The msb retains its original value ► The msb is replaced by the value of CF

Serial Port is also accessible via ***I/O*** ports , **COM 1** is accessible via ports 3F8-3FF while ***COM 2*** is accessible via 2F8 -2FF.

The first register at 3F8 is the ***Transmitter*** holding register if written to and the receiver ***buffer*** register if read from.

Other register of our interest include 3F9 whose ***Bit 0*** must be set to enable received data available interrupt and ***Bit 1*** must be set to enable transmitter holding register empty interrupt.
(Transmitter, COM 1, I/O ports , COM2. bit 0 , Buffer , 3FA)

There are three busses to communicate the processor and memory named as _____
address bus.,data bus and data bus.
addressing bus.,data bus and data bus.
address bus.,datamove bus and data bus.
address bus.,data bus and control bus..

The address bus is unidirectional and address always travels from processor to memory.
TRUE
FALSE

Control bus_____
is Not Important
is Important
bidirectional
unidirectional .

A memory cell is an n-bit location to store data, normally _____also called a byte
4-bit
8-bit
6-bit
80-bit

The number of bits in a cell is called the cell width._____ define the memory completely.
Cell width and number of cells
cell number and width of the cells,
width
Height

For memory we define two dimensions. The first dimension defines how many _____bits are there in a single memory cell.
parallel
Vertical
long
short

_____ operation requires the same size of data bus and memory cell width.
Normal
Best and simplest
first
None of the Given

Address always goes from
a. Processor to meory
b. Memory to processor
c. Memory to memory
d. None of the above
My Ok
Page # 9

The sourse register in OUT is
AL or AX
BL or BX
CL or CX
DL or DX

In the instruction mov word [es:160], 0x1230, 30 represents the character
A
B
0
1

Which of the following IRQ is cascading interrupt
IRQ 0
IRQ 1
IRQ 2
IRQ 3
Page # 114

SHR and SAL are same?
True
.False

mov ax,0 will set ZF flag
True
False

In 9 pin DB connector ,which pic is assigned to TD.
1
2
3
4

which is the special prefix used for repeating a block
rep
repeat
repb
repe

JA can not after cmp if unsigned destinition is greater than source
True
false

The value of a segment register when the processor is running under protected mode is called
segment descriptor segment selector global descriptor table protected register

FS and GS are two _____ in protected mode.
segment registers segment selectors stack pointers register pointe

Every bit of line status in serial port conveys _____ information.
different same partial full

There are total _____ bytes in a standard floppy disk.
1444k **1440k** 1280k 2480k

___ Decrements SP (the stack pointer) by two and then transfers a word from the source operand to the top of stack now pointed to by SP.
PUSH POP CALL MOV

PUSH increments SP (the stack pointer) by two and then transfers a word from the source operand to the top of stack now pointed to by SP.
True **False**

When the operand of DIV instruction is of 16-bits then implied dividend will be stored in_____
AX register **The concatenation of DX and AX**
The concatenation of ES and AX The concatenation of DS and BX

The parallel port connector is called?
BD-24 BD-25 **DB-25** DB-24

The instruction to call any software interrupt is
GO INT interrupt_number Call interrupt_number
INT interrupt_number Call INT interrupt_number

Peripheral address space is selected when which of the following instructions is given to the processor?
MOV DEC IN ADD

All the registers and stacks are saved in
Multitasking Multi Processing Function Call BIOS

When the subprogram finishes, the _____ retrieves the return address from the stack and transfers control to that location.
RET instruction CALL instruction POP instruction Jump instruction

Foreground and background parameter will be
32bits 16bits **8bits** 4bits

A 32 Bit processor has an accumulator of ---------
8 bit 16 bit **32 bit** 64 bit

RET is executed, it recovers the values from
Register **Stack** Data segment Code segment

The prevalent convention in most high level languages is stack clearing by the
Caller **Callee** RET Stack
My Ok Page # 40

After execution of JCXZ instruction CX will changed with flag affect.
CF OF DF **None of Above**

Execution of the instruction “mov word [ES : 0], 0x0741” will print
“A” appear on the top left of screen “A” appear on the top right of screen
“A” appear on the center of screen “A” appear on the bottom left of screen

if contains decimal -2 and BX contains decimal 2 then after the execution of instructions:
CMP AX, BX
JA label
Jump will be taken **Zero flag will set**

ZF will contain value -4 Jump will not be taken

Execution of the instruction “mov word [ES : 0], 0x1230” will print the character color will
Grean White Red Black

The source register in OUT is
AL or AX BL or BX CL or CX DL or DX
The source register in OUT and destination register in IN is AL or AX depending on which form is used.

In near jump we jump any where within a segment.
True False

The operations of placing items on the stack and removing them from there are called push and ret.
True **False**

Conditional jumps can only
Far Near **Short** All of the given

The root directory of floppy contains _____ fixed entries
64 256 128 **512**

Parameters clears from the stack by the
Caller callee caller and callee None of the given
My Ok Page # 74

if we apply NOT operation of bit 1 the answer is also 1
true **false**

RET do not pops the word at the top of the stack (pointed to by register SP) into the instruction pointer but increments SP by two.
True **False**
My Ok Page # 72

Stack is a data structure that behaves _____manner.
LIFO FIFO Both LIFO and FIFO None of the given

In the context of video services, if we want to get text mode chargen then which of the value place in AX
1110h 1010h 0011h 0001h

in the context of video services, if we want to set cursor position which of the following will be the value of AH
AH=01h **AH=02h** AH=03h AH=04h

There is no instruction to clear the
Trap flag Interrupt flag Direction flag None of the above

PCB stands for?
Process Control Block Process Clearing Block
Programable Counter Block Programs Control Block

The space where all the registers of a task are stored is called the
Control Block **Process control block** Stack Memory

The space where the current state is stored is called
Control block **Process control block** Stack Hard disk
My Ok Page # 140

The destination registers in OUT is ?
AL or AX BL or BX CL or CX DL or DX

The instruction used to read a character from the keyboard port is?
In al, 0x60 Out al, 0x60 In al, 0x80 Out al, 0x80

Each thread can have their own
execution area stack **memory** array

Which of the following interrupts is used for saving and restoring the registers
INT6 INT7 **INT8** INT0

from the following which is related to read a char from key board?
out al, 0x60 **in al, 0x60** out dx, al ou dx, 0x078

Video service is categories into 3 types of service.
True False

The instruction mov ax, 0
Will set the ZF **Will not set the ZF**
Is a mathematical instruction Is a logical instruction
My Ok Page # 32

After the execution of "PUSH AX" statement
AX register will reside on the stack **A copy of AX will go on the stack**
The value of AX disappear after moving on stack Stack will send an acceptance message

The data on which we want to perform some operation is called
Opcode **Operand** Operator Operation

Which of the following interrupt is a highest priority interrupt?
Key board interrupt **Timer interrupt** INT 2 INT 3

Suppose DH contains 10001010 and CL contains 3, what is the value of DH after the following instruction:
SHL DH, CL
01010000 10001010 00010100 01010111

The actual physical address representd by the segment-offset pair "AB01 FFFF" will be
1AB00 001AB **BB00F** F00BB

The OUT instruction uses _____ as source register.
AL or AX BL or BX CL or CX DL or DX

The memory address always move from_____
Processor to memory Memory to processor
Memory to peripheral Peripheral to processor

By executing which of the following instruction, the value in AX register becomes the half of previously stored value?
Shl AX, 1 **Shr AX, 1** NOT AX AND, AX, 0xFFFF

After the execution of following two instructions, what will happen?
PUSH AX POP DX
The value of DX will be at the top of the stack The value of AX will be at the top of the stack
The value of DX will be copied into AX **The value of AX will be copied into DX**
My Ok Page # 69

In the rotate right operation every bit moves one position to the right and the bit dropped from the right is inserted at the left end
The dropped bit is also copied in CF The dropped bit is also copied in AF
The dropped bit is also copied in ZF The dropped bit is not copied in any flag
My Ok Page # 53

"mov [bx], ax" moves the two bytes contents of AX register to the address contained in BX register in the current
Stack segment Code segment **Data segment** Extra segment
My Ok Page # 35

Which of the following is true?
In general the memory cell cannot be wider than data bus
Control bus is unidirectional
Memory can use the address bus to refer to certain register in processor
There is no relation between memory and data bus
My Ok Page # 10

Traditionally all the mathematical and logical operations are performed in
Code Segment register Data Segment register
Accumulator register Stack segment register
My Ok Page # 12

The word size of a processor is defined by the size of _____
Its accumulator register Address bus attached
Memory attached Control Bus
My Ok Page # 12

In A4FB:4872 Segment offset pair the physical address is (both segment and offset are in hexadecimal)
A4FB0 04872 **A9833** A4872

Relating to the stack in 8088 architecture which of the following statement is true?
Single word can not be pushed on the stack
Single word can not be popped from the stack
Single byte can not be popped from the stack
Single quad can be popped from the stack
My Ok Page # 68

_____ cannot predict which element the _____ needs, at a particular instant of time.
Control bus, Memory Processor, Control bus
Process, Memory **Memory, Processor**
My Ok Page # 9

When the instruction "CMP AX, BX" executed and after execution ZF is set, it indicates that
AX is greater **BX is greater**
Both AX and BX are equal ZF has no relation with CMP
My Ok

IBM PC has separate memory address space and peripheral address space. Memory address space is selected when _____ instruction is given to the processor.
► MOV ► DEC ► IN ► ADD
My Ok Page # 115

A thread can not be created_____
In static way In dynamic way
In static and dynamic way at the same time Manually

In DOS input buffer, the member of characters actually read on return is stored in _____ byte
Third Fourth First **second**
My Ok Page # 152

Segment wraparound occurs when during the effective address calculation_____ is generated
Carry Error Zero Parity
My Ok Page # 34

The value of AH register in the wire Graphics pixel service is_____
0Ch 0Bh 1Ch 2Ch
My Ok Page # 152

The bits of _____ register work independently. If combined all these bits then they are meaningless
Accumulator (AX) Instruction Pointer (IP) **Flag** Base
My Ok Page # 12

VBE stands for _____, as proposed by VESA (an organization)
Video BIOS Extensions Video BIOS Emergence
Video Binary Extensions Video Blocked Extensions
My Ok Page # 180

In computer Architecture, the protected mode is different from_____
Programming mode **Real Time mode** Visualization mode Memory Mode
My Ok

In Motorola 68K processors, _____ registers can hold addresses in indirect memory accesses.
A0-A7 B0-B7 C0-C7 D0-D7
My Ok Page # 191

In computer architecture, RISC stands for _____
Reversed Instruction Set computer Reversed Instruction System computer
Reduced instruction set computer Reduced Instruction System computer
My Ok Page # 192

"Far" jump makes intra _____ control possible
Register **Segment** Memory Code
My Ok Page # 46

Video services are exported via
INT 7 **INT 10** INT 9 INT 8
My Ok Page # 149

"INT 10 video-scroll up window" is type of video services used in which mode?
Numeric Graphics **Text** Audio
My Ok Page # 149

All possible types of Jumps in assembly language are
Short, far Short, near **Short, near, far** Short, near, far, long
My Ok Page # 46

The maximum memory iAPX88 can access is_____.
1MB 2MB 3MB 128MB
My Ok Page # 15

The first possible segment base value is _____
0000 0001 0010 0100
My Ok Page # 22

Technically IAPX88 stands for "_____ advanced processor Extensions 88."
Intel Integrated Intra Internal
My Ok Page # 14

In Left-Shift-Operation the left most bit _____
will drop **will go into CF** Will come to the right most will be always 1
My Ok Page # 52

Instruction "mov ax, bl" has a _____problem.
Size mismatch Value mismatch Operand mismatch Memory mismatch
My Ok Page # 30

In 9pin DB 9, which pin number is assigned to TD (Transmitted Data)?
► 1 ► 2 **► 3** ► 4
My Ok Page # 171

The jump "JC" is taken when
CF=1 CF=0 ZF=0 ZF=1
My Ok Page # 41

In 9 Pin DB-9, which pin number is assigned to DTR (Data Terminal Ready)?
1 2 3 **4**
My Ok

In 9pin DB 9, which pin number is assigned to RTS (Request to Send)?
5 6 **7** 8
My Ok Page # 171

Which of the following BIOS INT provides serial port services
INT 21 **INT14** INT10 INT8
My Ok Page # 171

The segment address of interrupt n will be at
nx^{4} nx^{4+1} **nx^{4+2}** nx^{4+3}
My Ok Page # 104

Which of the following interrupts in Non Maskable Interrput (NMI)?
INT 0 INT 1 INT 3 **INT 2**
My Ok Page # 105

_____ number of pin(s) of a processor is/are used by the external hardware to generate as interrupt
1 2 3 4
My Ok Page # 113

Far Jump is position relative
True **False**

How many characters standard ASCII has?
512 256 **128** 64

The purpose of MOVS instruction is
Move register to register Move register to a memory location
Move a memory location to register **Move memory to memory**

1 – Carrier Detect (CD)
2 – Received Data (RD)
3 – Transmitted Data (TD)
4 – Data Terminal Ready (DTR)
5 – Signal Ground
6 – Data Set Ready (DSR)
7 – Request to Send (RTS)
8 – Clear to Send (CTS)
9 – Ring Indicator (RI)

In 9 pin db 9 connector, which pin is assigned to RD(received data)
1 2 3 4
My Ok

In 9 pin db 9 connector, which pin is assigned to TD (transmitted data)
1 2 3 4
My Ok

In 9 pin 9 connector,which pin is assigned to signal ground
3 4 5 6
My Ok

In 9pin DB 9, RI (Ring Indicator) is assigned on pin number
► 6 ► 7 ► 8 **► 9**

In 9pin DB 9, which pin number is assigned to CD (Carrier Detect)?
► 1 ► 2 ► 3 ► 4

Page # 104

In 9pin DB 9, which pin number is assigned to DSR (Dataset Ready) ?
► 4 ► 5 **► 6** ► 7
page 146

In 9pin DB 9 CTS is assigned on pin number
6 7 **8** 9
Page # 164

In 9pin DB 9 CD is assigned on pin number
1 2 3 4
Page # 164

In 9pin DB 9 RD is assigned on pin number
1 **2** 3 4
Page # 164

In 9pin DB 9, which pin number is assigned to CTS (Clear To Send) ?
► 6 ► 7 **► 8** ► 9

In 9pin DB 9, Signal ground is assigned on pin number
► 4 **► 5** ► 6 ► 3

The operand of PUSH is called
Source operand Destination operand Stack operand Data operand
My ok Page #71

In shift instruction the destination can be
An 8-bit register only A register only
A memory location only A register or memory location

A fat32 file system directory entry in DOS consist of how many bytes?
16 24 32 64

Which register is generally used to specify the services number of an interrupt?
DX AX BX CX

In case of COM file, maximum length of parameters passed through command line can be…….
63 bytes **127bytes** 255 bytes 511 bytes

In case of COM File first command parameter is stored at _____ offset of program segment prefix.
0x80 0x82 0x84 0x86

Process of sending signals back and forth is called
Activity Hand-shaking Interruption **Time clicking**

Code Segment is associated to _____ register by default.
► IP ► SS ► BP ► CX
My Ok Page # 34

In string instruction, CX is always
Decremented by 1 Decremented by 2 **Incremented by 1** Incremented by 2

IBM AT has how many PICs (Programmable interrupt controller)
1 **2** 3 4
My Ok Page # 113

COM1 is connected with
IRQ1 IRQ3 **IRQ4** IRQ5

The maximum length of DOS command line parameters is
64 bits 127 bits **256 bits** 512 bits

_____ is one of the reasons due to which string instructions are used in 8088
Efficiency and accuracy Reduction in code size and accuracy
Reduction in code size and speed Reduction in code size and efficiency
My Ok Page # 91

We can access all the DOS services using
INT 0x21 INT 0x13 INT 0x10 INT 0x08
My Ok page # 153

In an indirect addressing mode the address of memory cell
Is placed in a register **Is directly accessed by instruction**
Is constant Is variable

In STOSB instruction, when DF is set, SI is
Incremented by 1 Incremented by 2 Decremented by 1 Decremented by 2

Processor informs the memory that it wants to read data, using
Address bus **Data Bus** Control bus It informs without using any bus

Memory cell width refers to _____
Number of bits in a cell
The maximum value that can be stored in a cell including sign-bit
The maximum value that can be stored in a cell excluding sign-bit
Address of that cell
My Ok Page # 10

In MUL instruction if the source operand is a byte then it is multiplied by register
AX **AL** CX DL
My Ok Page # 87

After the execution of REP instruction CX will be decremented then which of the following flags will be affected?
CF OF **DF** No flags will be affected
My Ok **Click Here**

The 'program segment prefix' for com files is of size:

64 bytes | 128 bytes | **256 bytes** | 512 bytes

Click Here

In the context of video services, if we want to write string then which of the value place in AH

10^{th} | 11^{th} | 12^{th} | **None of the above**

My Ok | Page # 150 | It's in 13^{th}

CALL instruction transfer the control

Permanently | **Temporarily**

Permanently when CALL is NEAR | Permanently when CALL is FAR

My Ok

7 – Blinking of foreground character
6 – Red component of background color
5 – Green component of background color
4 – Blue component of background color
3 – Intensity component of foreground color
2 – Red component of foreground color
1 – Green component of foreground color
0 – Blue component of foreground color

Which of the following are required for thread entry?

CS and DS | CS and IP | IP and general purpose registers | SS and SP

We can set the current file position in DOS using service number ____

0x38 | 0x40 | 0x42 | 0x43

On executing 0x21 0x3D, if file cant be opened then

CF will contain 1 | CF will contain 0

ZF will contain 1 | ZF will contain 0